UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,010	12/31/2001	Sompong Paul Olarig	H052617.1129US0	7506

1200 7590 05/13/2005

AKIN, GUMP, STRAUSS, HAUER & FELD
1111 LOUISIANA STREET
44TH FLOOR
HOUSTON, TX 77002

EXAMINER	
CHERY, MARDOCHEE	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,010	OLARIG ET AL.	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed on February 28, 2005, in response to PTO Office Action mailed on December 8, 2004. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. The newly added limitations introduced into dependent claim 13, and independent claims 16, and 25, do not remove the references from reading upon the claims.

a. As per claim 13, Leung et al. discloses "wherein each of the multiple target groups is addressable with a single base memory address", at col.4, lines 31-34 [the memory modules are independent, each with their own base address].

b. As per claim 16, Leung et al. discloses, "the initiator device configured to initiate" at col.7, lines 45-46, [all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106]. Further, Leung teaches, "wherein each of the plurality of target devices concurrently executes" at col.4, lines 41-49 [the memory module architectures allows parallel (concurrent) accesses and handle multiple memory accesses at the same time].

c. As per claim 25, Leung et al. discloses, "the initiator device configured to issue; the plurality of target devices configured to execute" at col.7, lines 45-46, [all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106].

3. Claims 1-31 have been presented for examination in this application. In response to PTO Office Action mailed on December 8, 2004, claims 1-4, 7-9, 12-18, 21, 25, and 29-31 have been amended. Claims 32-28 have been added. As a result, claims 1-38 are now pending in this application.

4. The objection to the Oath/Declaration has been withdrawn due to the amendment filed on February 28, 2005.

5. The rejection of claims 1-31, as in the Office Action mailed on December 8, 2004, is respectfully maintained and reiterated below for applicant's convenience.

Response to Arguments

6. Applicant's arguments on page 13, paragraph 2, filed on February 28, 2005, have been fully considered but they are not persuasive.

7. In response to applicant's argument that Leung et al. does not disclose "a multicast transaction", Examiner respectfully traverses applicant's arguments for the following reasons:

Examiner would like to point out that in Fig.17 and at col.7, lines 6-7, Leung et al. discloses "communication from masters to slaves is one-to-many (broadcast/multicast)"; col.23, lines 55-59, "broadcast-write and interleaved burst operations where different memory arrays in different modules are accessed simultaneously (concurrently)"; and col.24, lines 15-17, "write data is broadcast from I/O device 1704 to DASS bus 1702 and this data is simultaneously written into memory arrays 1730-1732".

Therefore, the rejection to claims 1-31 is respectfully maintained and reiterated below for Applicant's convenience.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In line 2, the limitation "wherein each of the multiple target groups is addressable with a single base memory address" renders the claim indefinite in that it does not clearly and specifically state whether "each of the multiple target groups" requires each, individually, "a single base memory address" or whether "a single base memory address" is addressing each (i.e. all) of the multiple target groups. The limitation as such is ambiguous.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1-23, and 25-31 are rejected under 35 U.S.C 102(e) as being unpatentable over Leung et al. (US 6,272,577).

As per claim 1, Leung et al. discloses a method for transacting between an initiator device and a plurality of target devices [*a memory device in which a single input data*

stream can be simultaneously written to multiple memory arrays; col.3, lines 63-65]; configuring the plurality of target devices to associate a portion of memory with a particular target device of the plurality of target devices [*a memory device which is organized into small memory arrays, wherein only one array is activated for each normal memory access*; col.3, lines 54-56]; sending a multicast transaction from the initiator device to the plurality of target devices [*a memory device in accordance with the present invention provides multiple commands, one after another, to different arrays*; col.25, lines 15-17]; executing the transaction when the transaction is received by the plurality of target devices according to the configuration of the target device [*since each memory module is a complete functional unit, the memory module architectures allows parallel processes and multiple memory module operations to be performed within different memory modules*; col.4, lines 42-45].

As per claim 2, Leung et al. discloses assigning a base memory address to be shared by the plurality of target devices [*a base address which identifies the memory module*; col.10, lines 20-23; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65]; and assigning a first portion of memory to a first target device of the plurality of target devices [*each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract].

As per claim 3, Leung et al. discloses the transaction is a read request for a block of stored data from memory [*a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27; *the address information comprises a base*

address of the memory device to be accessed; col.31, lines 12-14]; reading the base memory address from the read request *[each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract *; the memory modules are equipped with independent address and command decoders so that they function as independent units, each with their own base address*; col.4, lines 31-33]; initiating a read operation by the plurality of target devices assigned to the base memory address [*each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract; *a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27; *a base address which identifies the memory module*; col.10, lines 20-23]; fetching stored data from a portion of memory associated with each of the target devices, the data being concurrently fetched by each associated target device and sending the fetched data to the initiator device [*another multiple-array operation is an interleaved burst operation, in which a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27].

As per claim 4, Leung et al. discloses, the transaction is a write request for data to be stored in memory [*a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27]; reading the base memory address from the write request [*address information comprises a base address of the memory device to be accessed*; col.31, lines 13-14; *a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27]; initiating a write operation by the plurality of target devices assigned to the base memory address [*each memory module has*

independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed; abstract; *a base address which identifies the memory module*; col.10, lines 20-23]; and writing data of the write request to a portion of memory associated with each target device, the data being concurrently written by each associated target device[*another multiple-array operation is an interleaved burst operation, in which a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27].

As per claim 5, Leung et al. discloses, wherein the target devices comprise input/output Controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 6, Leung et al. discloses, the target devices comprise disk array controllers [Fig. 19; *controller 1920*].

As per claim 7, Leung et al. discloses, the plurality of target devices comprise a target group addressable with a single base memory address [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access*; col.5, lines 5-8].

As per claim 8, Leung et al. discloses, a plurality of target groups [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 9, Leung et al. discloses, a method for transacting data stored in memory between an initiator device and detecting a multicast transaction request [*multiple bank operations such as broadcast-write and interleaved access possible; a memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously*; col.5, lines 27-31]; accessing a first portion of memory by a first target device in response to the multicast transaction request [*when a memory read or write command is decoded, each memory module examines the communication ID of the command. All modules, except the module to which the command is addressed, go into an idle state until the read or write transaction is finished*; col.19, lines 42-47]; accessing a second portion of memory by a second target device concurrently with the access to the first portion of memory in response to the multicast transaction request [*a first field contains a base address which identifies the memory module by communication address. A second field contains an address which identifies the memory array within the memory module*. col.10, lines 21-25].

As per claim 10, Leung et al. discloses, the target devices comprise input/output Controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 11, Leung et al. discloses, the target devices comprise disk array Controllers [Fig. 19; *controller 1920*].

As per claim 12, Leung et al. discloses, wherein the first target device and the second target device are addressable with a single base memory address [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access*; col.5, lines 5-8].

As per claim 13, Leung et al. discloses, wherein a plurality of target devices are configured into multiple target groups wherein each of the multiple target groups is addressable with a single base memory address [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *the memory modules are independent, each with their own base address*; col.4, lines 31-34].

As per claim 14, Leung et al. discloses, multicast transaction comprises a multicast read
request [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46; *when a memory read or write command is decoded, each memory module examines the communication ID of the command*; col.19, lines 42-47].

As per claim 15, Leung et al. discloses, wherein the multicast transaction comprises a multicast write request [*multiple bank operations such as broadcast-write and*

interleaved-access; col.5, lines 27-29; *when a memory read or write command is decoded, each memory module examines the communication ID of the command*; col.19, lines 42-47; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65].

As per claim 16, Leung et al. discloses, a computer system for communicating between an initiator device and multiple target devices comprising [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46; *multiple bank operations such as broadcast-write and interleaved access possible; a memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously*; col.5, lines 27-31]; a communication bus [*memory device and allowing each memory module to have a communication address on the I/O bus system*; col.4, lines 54-56]; an initiator device coupled to the communications bus, the initiator device configured to initiate a transaction request [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46]; and a plurality of target devices coupled to the communications bus, wherein each of the plurality of target devices concurrently executes a portion of the transaction request [*the memory module architectures allows parallel (concurrent) accesses and handle multiple memory accesses at the same time*; col.4, lines 41-49; *a first field contains a base address which identifies the memory module by communication address. A second field contains an address which identifies the memory array within the memory module.* col.10, lines 21-25; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65; *a memory device in accordance with the present invention provides multiple commands, one after another, to different arrays*; col.25, lines 15-17].

As per claim 17, Leung et al. discloses the plurality of target device comprises input/output controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 18, Leung et al. discloses the plurality of target device comprises disk array controllers [Fig. 19; *controller 1920*].

As per claim 19, Leung et al. discloses a plurality of target devices are accessed with a single base memory address [*a first field contains a base address which identifies the memory module by communication address. A second field contains an address which identifies the memory array within the memory module*. col.10, lines 21-25].

As per claim 20, Leung et al. discloses the plurality of target devices comprise a target group [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 21, Leung et al. discloses a plurality of target groups [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 22, Leung et al. discloses the transaction is a multicast read request [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*;

col.7, lines 45-46; *when a memory read or write command is decoded, each memory module examines the communication ID of the command*; col.19, lines 42-47].

As per claim 23, Leung et al. discloses the transaction is a multicast write request [*multiple bank operations such as broadcast-write and interleaved-access*; col.5, lines 27-29; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65].

As per claim 25, Leung et al. discloses a computer system for multicast input/output transactions [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46; *multiple bank operations such as broadcast-write and interleaved access possible. A memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously*; col.5, lines 27-31]; a processor, a communications bus coupled to the processor [*the two processors can reside on the same bus using the same memory module*; col.10, lines 40-42]; an initiator device coupled to the communications bus, the initiator device configured to issue a multicast transaction, and a plurality of target devices coupled to the communications bus, the plurality of target devices configured to execute the multicast transaction with concurrent interleaved data responses [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46; *multiple bank operations such as broadcast-write and interleaved access possible. A memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously*; col.5, lines 27-31; *communication from masters to slaves is one-to-many (broadcast/multicast)*; Fig.17; col.7, lines 6-7; *broadcast-write and interleaved*

burst operations where different memory arrays in different modules are accessed simultaneously (concurrently); col.23, lines 55-59; *write data is broadcast from I/O device 1704 to DASS bus 1702 and this data is simultaneously written into memory arrays 1730-1732*; col.24, lines 15-17].

As per claim 26, Leung et al. discloses the target devices comprise input/output controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 27, Leung et al. discloses the target devices comprise disk array Controllers [Fig. 19].

As per claim 28, Leung et al. discloses the plurality of target devices comprise a target group, the target group addressable with a single base memory address [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access*; col.5, lines 5-8].

As per claim 29, Leung et al. discloses a plurality of target groups [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 30, Leung et al. discloses the multicast transaction is a multicast read request [*all memory transactions are initiated by either I/O module 104 or by devices connected*

to I/O bus 106; col.7, lines 45-46; *when a memory read or write command is decoded, each memory module examines the communication ID of the command*; col.19, lines 42-47].

As per claim 31, Leung et al. discloses the multicast transaction is a multicast write request [*multiple bank operations such as broadcast-write and interleaved-access*; col.5, lines 27-29; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65].

12. Claim 32 is rejected under 35 U.S.C 102(e) as being unpatentable over Gupta et al. (US 6,405,286).

As per claim 32, Gupta et al. discloses a computer comprising a memory [*computer systems with memory*; col.1, lines 24-25]; a controller configured to logically divide the memory into a plurality of interleaved memory regions [Fig. 2; *controller 22, interleaving table 24*]; and a plurality of devices, wherein each of the plurality of devices is associated with one of the interleaved memory regions and wherein each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction request [*interleaving to distribute memory across several banks so that multiple CPUs tend not to access the same memory banks; reads and writes may occur simultaneously*; col.6, lines 21-28].

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. in view of Carmichael et al. (US 5,864,712).

As per claim 24, Leung et al. discloses the claimed invention as detailed above in the previous paragraphs. However, Leung does not specifically teach the communications bus comprises a Peripheral Component Interconnect (PCI) bus as recited in the claim.

Carmichael discloses the communications bus comprises a Peripheral Component Interconnect (PCI) bus [*the bridge 36 may simply provide an extension of the processor's bus, or may buffer and extend the processor bus using an entirely different bus structure and protocol such as PCI*; col.6, lines 46-50] to provide an extension of the processor's bus and to buffer and extend the processor (col.6, lines 46-50).

Since the technology for implementing a data processing system using a PCI bus was well known in the art as evidenced by Carmichael, and since a PCI bus provides an extension of the processor's bus and to buffer and extend the processor, an artisan

would have been motivated to implement a PCI bus in the data processing system of Leung. Thus it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Leung to include a PCI bus to provide an extension of the processor's bus and to buffer and extend the processor (col.6, lines 46-50) as taught by Carmichael.

15. Claims 33-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta et al. (6,405,286) in view of Leung et al. (6,272,577).

As per claim 33, Gupta et al. discloses a method comprising dividing a section of memory into a plurality of interleaved memory regions [*interleaving to distribute memory across several banks;* col.6, lines 20-24]; associating the plurality of interleaved memory regions with a plurality of target devices [*interleaving memory banks associated with CPUs*; col.6, lines 21-23]; and executing a memory access that simultaneously involves each of the plurality of target devices accessing the interleaved memory region associated with each of the particular target devices [*multiple reads and writes may occur simultaneously; each memory bus can carry separate memory operations simultaneously with interleaving memory banks associated with CPUs;* col.12, lines 44-55].

Although Gupta et al. does not specifically teach associating the plurality of target devices with a single base memory address; Leung et al. discloses associating the plurality of target devices with a single base memory address [*the memory modules are*

independent, each with their own base address; col.4, lines 31-34] to allow parallel accesses and multiple memory module operations to be performed (col.4, lines 44-46).

Since the technology for implementing a data processing system with the plurality of target devices with a single base memory address was well known as evidenced by Leung, and since a single base memory address allows parallel accesses and multiple memory module operations to be performed, an artisan would have been motivated to implement this feature in the system of Gupta et al., because it was well known to allow parallel accesses and multiple memory module operations to be performed (col.4, lines 44-46) as taught by Leung et al..

As per claim 34, Gupta et al. discloses executing the memory access comprises executing a read operation [*executing memory access patterns such as read operations*; col.6, lines 24-27].

As per claim 35, Gupta et al. discloses executing the memory access comprises executing a write operation [*executing memory access patterns such as write operations*; col.6, lines 24-26].

As per claim 36, Gupta et al. discloses a tangible machine readable medium comprising code to initialize a plurality of devices [*BIOS routine can initialize the memory system*; col.11, lines 36-39]; and code to assign each of the plurality of devices a portion of an interleaved memory space [*interleaving memory banks associated with CPUs*; col.6, lines

21-23; *multiple reads and writes may occur simultaneously; each memory bus can carry separate memory operations simultaneously with interleaving memory banks associated with CPUs;* col.12, lines 44-55].

Although Gupta et al. does not specifically teach code to configure the plurality of devices to associate a base address with the plurality of devices, and tangible machine readable medium; Leung et al. discloses tangible machine readable medium [Fig.1]; and code to configure the plurality of devices to associate a base address with the plurality of devices [*a base address which identifies the memory module*; col.10, lines 20-23; *the memory modules are equipped with independent address and command decoders so that they function as independent units, each with their own base address*; col.4, lines 31-33] to allow parallel accesses and multiple memory module operations to be performed (col.4, lines 44-46).

Since the technology for implementing a data processing system with code to configure the plurality of devices to associate a base address with the plurality of devices was well known as evidenced by Leung, and since code to configure the plurality of devices to associate a base address with the plurality of devices allows parallel accesses and multiple memory module operations to be performed, an artisan would have been motivated to implement this feature in the system of Gupta et al.. Thus it would have been obvious to modify the system of Gupta et al. to include code to configure the plurality of devices to associate a base address with the plurality of devices because it was well known to allow parallel accesses and multiple memory module operations to be performed (col.4, lines 44-46) as taught by Leung et al..

As per claim 37, Gupta et al. discloses code to issue a single read command comprising the base address [*memory bus allows memory read operations with each memory bus carrying a single memory operation*; col.6, lines 11-14; *the memory modules are independent, each with their own base address*; col.4, lines 31-34; *program code to perform read operations*; col.6, lines 53-54]; code to recognize the base address as associated with the plurality of devices [*a base address which identifies the memory module*; col.10, lines 20-23; *program code to perform operations*; col.6, lines 53-54]; code to simultaneously execute a plurality of memory requests involving the plurality of devices [*reads and writes occur simultaneously*; col.6, lines 21-28; *program code to perform read operations*; col.6, lines 53-54]; code to receive data from the plurality of devices [*each memory receives data as it is read*; col.8, lines 11-12; *program code to perform read and write operations*; col.6, lines 53-55]; and code to write the received data to a communications bus [*unit to initiate write operations to memory modules*; col.8, lines 14-16].

As per claim 38, Gupta et al. discloses Code to issue a write command comprising the base address [*write operations with each memory bus carrying a single memory operation*; col.6, lines 12-15; *the memory modules are independent, each with their own base address*; col.4, lines 31-34; *program code to perform read and write operations*; col.6, lines 53-55]; code to recognize the base address as associated with the plurality of devices [*the memory modules are independent, each with their own base address*; col.4, lines 31-34; *program*

code to perform read and write operations; col.6, lines 53-55]; and code to simultaneously write to the plurality of devices [*reads and writes occur simultaneously*; col.6, lines 21-28].

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gupta et al.	6,405,286
Leung et al.	6,272,577
Leung et al.	6,754,746
Howard	5,950,218
Carmichael et al.	5,864,712

18. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

19. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 11, 2005

MC

Mardochee Chery
Examiner
AU2188

Pierre M. Vital

Pierre M. Vital
Primary Examiner
AU2188